All

thickness of insulator film to form a transition metal window, whereby the size of said first area of crystallized film is influenced.

Claim 74 (New). A TFT structure as in claim 71 in which said insulator film material is selected from the group consisting of silicon dioxide and silicon nitride.

Claim 75 (New). A TFT structure as in claim 61 in which said film of semiconductor material has a thickness in the range from 200 to 10,000 Å.

Please cancel claims 1 through 31.

REMARKS

This Preliminary Amendment accompanies a divisional patent application. Applicants herein cancel method claims 1-31. This divisional application pursues device claims 32-60 together with newly added claims 61-75. In addition, several typographical errors in the specification have been corrected.

On pages 16-20 below the changes to the specification made herein are set forth with all changes indicated. Page 22 below contains the changes to the claims made herein with all changes indicated. Pages 24-31 below contain a full set of the claims pending in this application, incorporating all amendments made herein. Following page 32 are

replacement pages for specification page nos. 1, 8, 11, 13, 15, 18, 21, and 22 incorporating all changes made to those pages herein.

Applicants respectfully request entry of this Preliminary Amendment and consideration of the application as amended.

Respectfully submitted,

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David C. Ripma
Registration No. 27,672

David C. Ripma, Patent Counsel
Sharp Laboratories of America, Inc.
5750 N.W. Pacific Rim Blvd.
Camas, WA 98607

Telephone: (360) 834-8754
Facsimile: (360) 817-8505

The following pages 16-20 of the present Preliminary Amendment Accompanying Divisional Application Under 37 C.F.R. § 1.53(b), dated 1/8/02, indicates the changes to the specification made herein

In the amended claims deleted material is indicated in brackets [ ] and added material is underlined.

At page 1, line 4, the following section was added (underlining omitted):

Cross Reference to Related Applications

This application is a divisional of application Serial No. 09/118,307, filed July 16, 1998, entitled "Single Crystal TFT From Continuous Transition Metal Delivery Method," invented by Maekawa et al.

The paragraph on page 8, lines 9-16, was changed as follows:

An ion implantation method implants transition metal within a rectangular window having a width in the range from 20 to 50 microns and a length of at least 50 microns. The exact length is dependent on the number of crystallization sites to be formed. In this manner, a concentration of transition metal no more than 2 x 10^{19} atoms per cubed centimeter, and a density of transition metal nucleus sites no more than 1 x 10^{7} per square [centimeters] centimeter is maintained. The distance between transition metal nucleus sites is no less than 2 microns.

The paragraphs on page 11, lines 8-27, were changed as follows:

Fig. 2 illustrates transistor 10 of Fig. 1 following an annealing process. Transition metal 16 has moved along a lateral growth front out from silicon areas 12a and 12b. At the finish of the annealing process the two growth fronts intersect in the center of the channel region, labeled [12d] 12c. The silicon regions behind the growth front of transition metal 16 have been

transformed with transition metal 16 into crystallized silicon 18. That is, silicon areas 12a, 12b, and parts of 12c have been crystallized. Although the bulk of silicon areas 12a and 12b may be crystallized silicon, devoid of transition metal semiconductor compounds, such as silicide, the limited source of amorphous silicon in area 12c and the intersecting fronts may result in an area of silicide in channel region [12d] 12c.

Typically, source drain areas 12a and 12b are amorphized in response to large doping implants in the formation of active source/drain regions. When source/drain regions 12a and 12b are annealed again for implant activation, a danger exists that transition metal grains 16 in channel region [12d] 12c could migrate back into the amorphous source/drain regions 12a and 12b. The presence of transition metal grains in source/drain regions 12a and 12b increases leakage current as transition metal 16 tends to act as a short across the reverse bias junction.

The paragraph on page 13, lines 17-27, was changed as follows:

Fig. 6 depicts [of] transistor 200 of Fig. [4] 5 following annealing. Amorphous first film 202 is annealed to form a first area of crystallized first film 208. First area 208 (cross-hatched) is a single grain of crystal. In subsequent steps a pattern is etched into first area 208 of crystallized first film to form the source/drain regions 209 (double cross-hatched), whereby a transistor is formed having high electron mobility and low leakage current in the transistor active areas. Areas 210 and 212 are single crystal grains for the fabrication of neighboring transistors. In some aspects of the invention, the subsequently formed transistors overlie neighboring areas of crystallized

film, such as areas 208, 210, and 212. In those circumstances a transistor is formed from multiple crystal grains.

The paragraph on page 15, lines 9-15, was changed as follows:

Transition metal 204 doping is selected from the group consisting of ion implantation and CVD deposition methods. The first concentration of transition metal is less than 2×10^{19} atoms per cubed centimeter, and the first density of transition metal nucleus sites are less than 1×10^{7} per square [centimeters] centimeter. Only three nucleation sites are shown in Figs. 5-7 for the purpose of clarity. First distance 206 between transition metal nucleus sites 204 is no less than 2 microns.

The paragraph beginning on page 17, line 25, and continuing through page 18, line 2, was changed as follows:

Fig. 12c depicts the concentration of Ni atoms 306 in the later stages of annealment. A nucleation site 204 is formed in the center of window 308, with relatively low concentrations of Ni atoms 306 [is] in the remaining area of window 308.

The paragraph on page 18, lines 8-14, was changed as follows:

Fig. 13 depicts further fabrication steps of transistor 300 of Fig. 10 after annealing and transition metal semiconductor compound 316 removal. An oxide layer 320 overlies the channel region 322. A gate electrode 324 overlies oxide layer [322] 320. In some aspects of the invention, phosphorous 326 is implanted into source 328 and drain 330 regions. Alternately, boron 326 is implanted. Annealing is performed to activate implanted species 326.

The paragraph on page 21, lines 12-16, was changed as follows:

In some aspects of the invention, Step 404 includes a first concentration of transition metal no more than 2 x 10^{19} atoms per cubed centimeter, and the first density of transition metal nucleus sites no more than 1 x 10^{7} per square [centimeters] centimeter. Step 404 includes a first distance between transition metal nucleus sites of no less than 2 microns.

The paragraph on page 22, lines 17-27, was changed as follows:

Fig. 16 is a flowchart illustrating another aspect of a method of forming a crystallized film with large crystal grains. Step 500 provides a semiconductor film and a transition metal. Step 502 heats the semiconductor film to a temperature in the range from 700 to 750 degrees C. Step 504 heats the semiconductor film for a duration in the range from 1 to 5 minutes. Step 506 supplies a transition metal concentration of no more than 2 x 10^{19}

atoms/cm^3. Step 508 maintains a transition metal nucleation site density of no more than 1 x $10^7/cm^2$. Step 510 maintains a distance between transition metal nucleation sites of no less than 2 microns. Step 512 forms large grains of crystallized semiconductor film corresponding to the distance between transition metal nucleation sites.--

The following page 22 of the present Preliminary Amendment Accompanying Divisional Application Under 37 C.F.R. § 1.53(b), dated 1/8/02, indicates the changes to the claims made herein

In the amended claims deleted material is indicated in brackets [ ] and added material is underlined.

Claim 46 was changed as follows:

Claim 46 (Amended). A TFT as in claim 32 in which said amorphous first film is doped with said transition metal to said first density of transition metal nucleus sites is less than 1 x 10^7 per square [centimeters] centimeter.

The following pages 24-31 of the present Preliminary Amendment Accompanying Divisional Application Under 37 C.F.R. § 1.53(b), dated 1/8/02, contains a full set of the pending claims in the present divisional application incorporating all changes to the claims made herein

32. A first thin-film transistor (TFT) comprising source/drain and channel regions of a single grain of crystallized first film material formed from doping an amorphous first film with a transition metal through a transition metal window at a first concentration, first density of nucleation sites, and a first distance between nucleation sites, annealing said amorphous first film to form a first area of crystallized first film which is a single grain of crystal, and etching a pattern in said first area of crystallized first film to form the source/drain regions, whereby a transistor is formed having high electron mobility and low leakage current in the transistor active areas.

33. A TFT as in claim 32 further comprising:

a gate electrode;

a gate oxide layer overlying said gate electrode; and

in which said gate electrode and gate oxide layer are deposited before said first film, whereby a bottom gate TFT is fabricated.

34. A TFT as in claim 32 further comprising:

a gate oxide layer overlying said channel region; and

a gate electrode overlying said gate oxide layer, whereby a top gate TFT is fabricated.

35. A TFT as in claim 32 in which said first film material is selected from the group consisting of silicon, germanium, silicon carbide, and silicon-germanium compounds.

36. A TFT as in claim 32 in which the transition metal is selected from the group consisting of Al, Ni, Ti, Co, and Pd.

37. A TFT as in claim 32 in which the temperature is ramped-up to the annealing temperature at a rate greater than 5 degrees C per second, whereby the first film is annealed at the intended temperature for larger crystal grains.

38. A TFT as in claim 32 in which the annealing is performed with an RTA process at a temperature in the range from 600 to 800 degrees C, for a time duration in the range from 1 second to 15 minutes.

39. A TFT as in claim 38 in which the annealing is performed with an RTA process at a temperature in the range from 700 to 750 degrees C, for a time duration in the range from 1 to 5 minutes.

40. A TFT as in claim 39 in which the annealing is performed with an RTA process at a temperature at approximately 720 degrees C and a time duration of approximately 2 minutes.

41. A TFT as in claim 32 in which transition metal semiconductor compound surrounding said first area of crystallized first film is removed when said source/drain regions are defined, whereby said crystallized film is cleaned of materials which promote high leakage currents.

42. A TFT as in claim 32 in which said transition metal is doped within a rectangular window overlying said first area of crystallized film, having a width in the range from 20 to 50 microns.

43. A TFT as in claim 32 in which said transition metal is doped within a rectangular window overlying said first area of crystallized film, having a length in the range from 60 to 150 microns.

44. A TFT as in claim 32 wherein at least a second TFT is formed adjoining the first TFT, in which at least a second area of crystallized first film is formed adjoining said first area of crystallized first film, and in which said transition metal is doped within a rectangular window overlying said first and second areas of crystallized film having a width in the range from 20 to 50 microns and a length of 50 microns, or greater.

45. A TFT as in claim 32 in which said amorphous first film is doped with said transition metal to said first concentration of transition metal less than 2×10^{19} atoms per cubed centimeter.

46. A TFT as in claim 32 in which said amorphous first film is doped with said transition metal to said first density of transition metal nucleus sites is less than 1×10^{7} per square centimeter.

47. A TFT as in claim 32 in which the first distance between said transition metal nucleus sites is no less than 2 microns.

48. A TFT as in claim 32 in which the ratio of said transition metal window area to said first area of crystallized film is in the range from 1:1 to 1:3.

49. A TFT as in claim 32 in which said first area of crystallized first film is in the range from 20 to 8,000 square microns (μ^2).

50. A TFT as in claim 32 in which transition metal doping is selected from the group consisting of ion implantation and CVD deposition.

51. A TFT as in claim 32 in which said transition metal doping occurs, at least partially, simultaneously with the annealing of said first film, whereby said transition metal is continually introduced during the annealing process to support the lateral growth of crystallization.

52. A TFT as in claim 51 in which an insulator film having a first thickness is deposited over said amorphous first film, with said transition metal being deposited overlying said insulator film, and in which said transition metal diffuses through said insulator film into said amorphous first film first thickness during annealing, whereby the formation of said transition metal nucleuses is controlled.

53. A TFT as in claim 52 in which said transition metal overlying said insulator film is selectively etched before annealing to form said transition metal window, whereby the size of said first area of crystallized first film is influenced.

54. A TFT as in claim 52 in which said insulator film is deposited with an initial thickness and selectively etched to form an area having a first thickness, less than the initial thickness, and in which said transition metal is deposited over said first thickness of insulator film to form said transition metal window, whereby the size of said first area of crystallized film is influenced.

55. A TFT as in claim 54 in which said initial thickness is 500 Å, or greater.

56. A TFT as in claim 52 in which said insulator film has a first thickness in the range from 10 to 100 Å.

57. A TFT as in claim 52 in which said insulator material is selected from the group consisting of silicon dioxide and silicon nitride.

58. A TFT as in claim 52 in which said transition metal is deposited with a thickness in the range from 10 to 1000 Å.

59. A TFT as in claim 32 further comprising a glass substrate, and in which said crystallized first film is formed overlying said glass substrate.

60. A TFT as in claim 32 in which said amorphous first film has a thickness in the range from 200 to 10,000 Å.

61. A thin-film transistor (TFT) structure, comprising:

a film of semiconductor material formed on a transparent substrate, said semiconductor material including a first area in which the semiconductor material is crystallized around selected transition metal nucleation sites;

source/drain and channel regions formed in said first area; and

the distance between said transition metal nucleation sites is no less than 2 microns, whereby a transistor is formed having high electron mobility and low leakage current in the transistor active areas.

62. A TFT structure as in claim 61 further including a gate electrode formed on said first area and a gate oxide layer overlying said gate electrode, in which said gate electrode and gate oxide layer are deposited before said first film, whereby a bottom gate TFT is fabricated.

63. A TFT structure as in claim 61 further including a gate oxide layer overlying said channel region in said first area and a gate electrode overlying said gate oxide layer, whereby a top gate TFT is fabricated.

64. A TFT structure as in claim 61 in which said film of semiconductor material is selected from the group consisting of silicon, germanium, silicon carbide, and silicon-germanium compounds.

65. A TFT structure as in claim 61 in which the transition metal nucleation sites include transition metal selected from the group consisting of Al, Ni, Ti, Co, and Pd.

66. A TFT structure as in claim 61 in which a transition metal semiconductor compound surrounding said first area of crystallized semiconductor material is removed when said source/drain regions are defined, whereby said crystallized semiconductor material is cleaned of materials which promote high leakage currents.

67. A TFT structure as in claim 61 in which said first area is a rectangular window overlying an area of said semiconductor material which is crystallized, said first area having a width in the range from 20 to 50 microns.

68. A TFT structure as in claim 61 in which said film of semiconductor material in said first area is doped with a transition metal to a concentration of less than 2×10^{19} atoms per cubed centimeter.

69. A TFT structure as in claim 61 in which said film of semiconductor material in said first area is doped with a transition metal to a density of transition metal nucleus sites of less than 1×10^{7} per square centimeter.

70. A TFT structure as in claim 61 in which said first area of crystallized semiconductor material has an area in the range from 20 to 8,000 square microns (μ^2).

71. A TFT structure as in claim 61 in which the concentration of transition metal nucleuses in said first area is controlled by depositing an insulator film having a first thickness over said film of semiconductor

material, and in which transition metal is deposited overlying said insulator film such that said transition metal diffuses through said insulator film into said semiconductor material during annealing.

72. A TFT structure as in claim 71 in which said transition metal overlying said insulator film is selectively etched before annealing to form said transition metal window, whereby the size of said first area of crystallized first film is influenced.

73. A TFT structure as in claim 71 in which said insulator film is deposited with an initial thickness and selectively etched to form an area having a first thickness, less than the initial thickness, in said first area, and in which said transition metal is deposited over said first thickness of insulator film to form a transition metal window, whereby the size of said first area of crystallized film is influenced.

74. A TFT structure as in claim 71 in which said insulator film material is selected from the group consisting of silicon dioxide and silicon nitride.

75. A TFT structure as in claim 61 in which said film of semiconductor material has a thickness in the range from 200 to 10,000 Å.

The following are replacement pages for specification page nos. 1, 8, 11, 13, 15, 18, 21, and 22 incorporating all changes made thereto in the present Preliminary Amendment Accompanying Divisional Application Under 37 C.F.R. § 1.53(b), dated 1/8/02

SINGLE CRYSTAL TFT FROM CONTINUOUS TRANSITION METAL DELIVERY METHOD

Cross Reference to Related Applications

This application is a divisional of application Serial No. 09/118,307, filed July 16, 1998, entitled "Single Crystal TFT From Continuous Transition Metal Delivery Method," invented by Maekawa et al.--

Background and Summary of the Invention

This invention relates generally to thin-film transistor (TFT) processes and fabrication, and more particularly, to a TFT polycrystalline film, and method of forming large grain sheets of polycrystalline silicon using transition metals semiconductor compounds, such as nickel silicide, to induce the crystallizing of an amorphous film through lateral growth from selective locations on a silicon wafer.

The demand for smaller electronic consumer products with higher resolution displays, spurs continued research and development in the area of liquid crystal displays (LCDs). The size of LCDs can be decreased by incorporating the large scale integration (LSI) and very large scale integration (VLSI) driver circuits, presently on the periphery of LCDs, into the LCD itself. The elimination of externally located driving circuits and transistors will reduce product size, process complexity, a number of process steps, and ultimately the price of the product in which the LCD is mounted.

The primary component of the LCD, and the component that must be enhanced for further LCD improvements to occur, is the thin-film transistor (TFT). TFTs are typically fabricated on a transparent substrate such as quartz, glass, or even plastic. TFTs are used as switches to allow the various pixels of the LCD to be charged in response to the driver circuits. TFT performance will be improved, and driver circuit functions incorporated into TFTs, by increasing the electron mobility in the TFT devices. Increasing the electron mobility of a transistor results in a

b) implanting or depositing (alternatively referred to as doping) a first concentration of transition metal on the amorphous film, to form a first density of transition metal nucleus sites, with the nucleation sites being separated by a first distance, whereby a low density of nucleation sites is formed; and

c) annealing to form large areas of single grain crystallized film, whereby a crystallized film is prepared for the fabrication of a high electron mobility transistors.

An ion implantation method implants transition metal within a rectangular window having a width in the range from 20 to 50 microns and a length of at least 50 microns. The exact length is dependent on the number of crystallization sites to be formed. In this manner, a concentration of transition metal no more than 2×10^{19} atoms per cubed centimeter, and a density of transition metal nucleus sites no more than 1×10^{7} per square centimeter is maintained. The distance between transition metal nucleus sites is no less than 2 microns.

A diffusion layer is used in a continual transition metal delivery system aspect of the invention. Then, Step b) is performed, at least partially, simultaneously with the performance of Step c). In this manner, transition metal is continually introduced during the annealing process to support the lateral growth of crystallization, without increasing the metal concentration above the defined minimum. An insulator film having a first thickness is deposited over the amorphous film. The transition metal is deposited over the insulator film and selectively etched to form a predetermined window size. Alternately, the insulator film is selectively thinned to define a window with a first thickness before the deposition of metal. Either way, Step c) includes the diffusion of

layer 16 to cover surrounding areas 14, however, in the self-aligning silicide (salicide) process transition metal 16 only reacts with silicon. Therefore, metal 16 is not shown overlying areas 14. Transition metal 16 is also not shown overlying channel region 12c, since channel region 12c is usually covered by a gate oxide layer, and even a gate electrode at this stage of the process. Neither the gate oxide layer, nor gate electrode is shown for the sake of clarity.

Fig. 2 illustrates transistor 10 of Fig. 1 following an annealing process. Transition metal 16 has moved along a lateral growth front out from silicon areas 12a and 12b. At the finish of the annealing process the two growth fronts intersect in the center of the channel region, labeled 12c. The silicon regions behind the growth front of transition metal 16 have been transformed with transition metal 16 into crystallized silicon 18. That is, silicon areas 12a, 12b, and parts of 12c have been crystallized. Although the bulk of silicon areas 12a and 12b may be crystallized silicon, devoid of transition metal semiconductor compounds, such as silicide, the limited source of amorphous silicon in area 12c and the intersecting fronts may result in an area of silicide in channel region 12c.

Typically, source drain areas 12a and 12b are amorphized in response to large doping implants in the formation of active source/drain regions. When source/drain regions 12a and 12b are annealed again for implant activation, a danger exists that transition metal grains 16 in channel region 12c could migrate back into the amorphous source/drain regions 12a and 12b. The presence of transition metal grains in source/drain regions 12a and 12b increases leakage current as transition metal 16 tends to act as a short across the reverse bias junction.

deposition allows control over the areas in which the metal-semiconductor compounds reside. But selective distribution required higher concentrations of metal. High concentrations of metal result in closely grouped nucleation sites and, ultimately, same crystal grains. The present invention permits selective placement of transition metal and low transition metal concentrations.

Figs. 5-7, 9-11, and 13-14 depict steps in the formation of at least a single completed thin-film transistor (TFT) comprising source/drain and channel regions of a single grain of crystallized first film material. Fig. 5 is a plan view of transistor 200. An amorphous first semiconductor film 202 is doped with a transition metal at a first concentration, first density of nucleation sites 204, and a first distance 206 between nucleation sites 204. First film material 202 is selected from the group consisting of silicon, germanium, silicon carbide, and silicon-germanium compounds. The transition metal of nucleation sites 204 is selected from the group consisting of Al, Ni, Ti, Co, and Pd.

Fig. 6 depicts transistor 200 of Fig. 5 following annealing. Amorphous first film 202 is annealed to form a first area of crystallized first film 208. First area 208 (cross-hatched) is a single grain of crystal. In subsequent steps a pattern is etched into first area 208 of crystallized first film to form the source/drain regions 209 (double cross-hatched), whereby a transistor is formed having high electron mobility and low leakage current in the transistor active areas. Areas 210 and 212 are single crystal grains for the fabrication of neighboring transistors. In some aspects of the invention, the subsequently formed transistors overlie neighboring areas of crystallized film, such as areas 208, 210, and 212. In those circumstances a transistor is formed from multiple crystal grains.

concentration of 2 x 10^{19} atoms per cubed centimeter typically lead to an increase in the transition metal nucleation site density above 1 x 10^{7} per square centimeter. At these higher densities, the spacing between nucleation sites decreases, so that smaller crystal grain are formed. However, when the concentration of transition metal falls too far below 2 x 10^{19} atoms per cubed centimeter, there is insufficient metal to support the lateral growth of transition metal semiconductor compounds, such as di-silicide, during annealment.

Transition metal 204 doping is selected from the group consisting of ion implantation and CVD deposition methods. The first concentration of transition metal is less than 2 x 10^{19} atoms per cubed centimeter, and the first density of transition metal nucleus sites are less than 1 x 10^{7} per square centimeter. Only three nucleation sites are shown in Figs. 5-7 for the purpose of clarity. First distance 206 between transition metal nucleus sites 204 is no less than 2 microns.

Fig. 8 is a graph detailing the relationship between transition metal deposition and crystal grain size. To alleviate the above-mentioned transition metal concentration problem, a continuous transition metal delivery system was developed. That is, transition metal implanting occurs, at least partially, simultaneously with the annealing of said first film, whereby said transition metal is continually introduced during the annealing process to support the lateral growth of crystallization. Fig. 8 shows that at a nucleation density of 1 x $10^{7}/cm^{2}$, the concentration of Ni atoms is approximately 2 x 10^{19} atoms/cm^{3}, and the nearest neighbor distance (N.N.D.) is 2 microns.

Annealing is performed with an RTA process at a temperature in the range from 600 to 800 degrees C, for a time duration

of window 308, with relatively low concentrations of Ni atoms 306 in the remaining area of window 308.

Returning briefly to Fig. 6, transition metal semiconductor compounds 316 surrounding first area 208 of crystallized first film are removed when source/drain regions 209 are defined after annealing, whereby crystallized film is cleaned of materials which promote high leakage currents.

Fig. 13 depicts further fabrication steps of transistor 300 of Fig. 10 after annealing and transition metal semiconductor compound 316 removal. An oxide layer 320 overlies the channel region 322. A gate electrode 324 overlies oxide layer 320. In some aspects of the invention, phosphorous 326 is implanted into source 328 and drain 330 regions. Alternately, boron 326 is implanted. Annealing is performed to activate implanted species 326.

Fig. 14 depicts TFT 300 of Fig. 13 following the removal of oxide layer 320. A gate oxide layer 332 remains, gate electrode 324 overlies gate oxide layer 332. A dielectric interlevel 334 is deposited over transistor 300. Contact holes 336 are defined through dielectric interlevel 334 and metal 338 is deposited in contact holes 336 so that an electrical interface is made to source/drain regions 328/330. In this manner, a top gate TFT is fabricated. Alternately, but not shown, a bottom gate TFT is fabricated by depositing gate electrode 324 and gate oxide layer 332 before deposited first film 202, as is well known in the art.

Fig. 15 is a flowchart illustrating steps in a method for forming large crystal grains. Step 400 provides an amorphous film. Step 402 deposits a layer of the amorphous first film. Step 402 includes an amorphous first film selected from the group consisting of silicon,

transition metal over the insulator film first thickness, whereby the size of the first area of crystallized film is influenced.

Step 406 includes the first area of crystallized first film being in the range from 20 to 8,000 square microns (μ^2). Typically, Step 402b includes the transition metal window being a rectangle having a width in the range from 20 to 50 microns and a length in the range from 60 to 150 microns, as explained above with the ion implantation process. Likewise, when Step 406 includes forming at least a second area of crystallized first film, Step 402b includes the transition metal window being a rectangle having a width in the range from 20 to 50 microns and a length of 50 microns, or greater.

In some aspects of the invention, Step 404 includes a first concentration of transition metal no more than 2×10^{19} atoms per cubed centimeter, and the first density of transition metal nucleus sites no more than 1×10^{7} per square centimeter. Step 404 includes a first distance between transition metal nucleus sites of no less than 2 microns.

In some aspects of the invention, further steps, precede Step 406. Step 404a ramps-up the temperature to the annealing temperature of Step 406 at a rate greater than 5 degrees C per second, whereby the first film is annealed at the intended temperature of Step 406 for a larger crystal grain.

Step 406 includes using a Rapid Thermal Annealing (RTA) process at a temperature in the range from 600 to 800 degrees C, and a time duration in the range from 1 second to 15 minutes. In one aspect of the invention, Step 406 includes using a Rapid Thermal Annealing (RTA) process at a temperature in the range from 700 to 750 degrees C, and a time duration in the range from 1 to 5 minutes. In another aspect of the

invention, Step 406 includes using a Rapid Thermal Annealing (RTA) process at a temperature of approximately 720 degrees C and a time duration of approximately 2 minutes.

When a TFT is be fabricated, Step 400 provides a glass substrate and a barrier layer overlying the glass substrate. Then, Step 402 includes depositing the first film overlying the barrier layer and glass substrate. Further steps (not shown), are involved. When a top gate transistor is to be performed, additional steps follow Step 406. Step 406b forms transistor source, drain, and channel regions within the first area of crystallized film, whereby the source, drain, and channel regions are formed from a single crystal grain, without the presence of transition metal semiconductor compounds. Step 406c forms a gate oxide layer. Step 406d forms a gate electrode. Step 406e implants doping species. Step 406f anneals to activate the implanted species, whereby a top gate TFTs is formed. When a bottom gate TFT is formed, Steps 406c and 406d precede Step 402, as is well known in the art.

Fig. 16 is a flowchart illustrating another aspect of a method of forming a crystallized film with large crystal grains. Step 500 provides a semiconductor film and a transition metal. Step 502 heats the semiconductor film to a temperature in the range from 700 to 750 degrees C. Step 504 heats the semiconductor film for a duration in the range from 1 to 5 minutes. Step 506 supplies a transition metal concentration of no more than 2×10^{19} atoms/cm^3. Step 508 maintains a transition metal nucleation site density of no more than 1×10^7/cm^2. Step 510 maintains a distance between transition metal nucleation sites of no less than 2 microns. Step 512 forms large grains of crystallized semiconductor film corresponding to the distance between transition metal nucleation sites.